APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,697	01/25/2002	Chao-Chen Kuo	02110-URSX	9049

33804   7590   07/15/2005

SUPREME PATENT SERVICES
POST OFFICE BOX 2339
SARATOGA, CA 95070

EXAMINER
WILLIAMS, JEFFERY L

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	**Applicant(s)**
Office Action Summary	10/057,697	KUO, CHAO-CHEN
	Examiner	**Art Unit**	
	Jeffery Williams	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 January 2002</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-6</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-6</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>25 January 2002</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

1   **DETAILED ACTION**

2

3   *Claim Rejections - 35 USC § 112*

4

5   The following is a quotation of the second paragraph of 35 U.S.C. 112:

6   The specification shall conclude with one or more claims particularly pointing out and distinctly
7   claiming the subject matter which the applicant regards as his invention.
8
9   **Claims 1 – 6 are rejected under 35 U.S.C. 112, second paragraph, as being**

10   **indefinite for failing to particularly point out and distinctly claim the subject**

11   **matter which applicant regards as the invention.**

12   The terms "proper" and "easily" in claim 1 are relative terms that render the claim

13   indefinite. The terms "proper" and "easily" are not defined by the claim, the specification

14   does not provide a standard for ascertaining the requisite degree, and one of ordinary

15   skill in the art would not be reasonably apprised of the scope of the invention.

16

17   Regarding claims 2 – 6, they are rejected by virtue of their dependency upon

18   claim 1.

19

20   *Claim Rejections - 35 USC § 103*

21

22   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

23   obviousness rejections set forth in this Office action:

24   (a) A patent may not be obtained though the invention is not identically disclosed or described as set
25   forth in section 102 of this title, if the differences between the subject matter sought to be patented and

1   the prior art are such that the subject matter as a whole would have been obvious at the time the
2   invention was made to a person having ordinary skill in the art to which said subject matter pertains.
3   Patentability shall not be negatived by the manner in which the invention was made.
4

5   **Claims 1 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over**

6   **Admitted Prior Art as disclosed by Applicant in view of Babcock, "Control of a**

7   **Function of a Computer Other Than a Power Supply Function Using a System**

8   **Power Switch", U.S. Patent 5,845,136.**

9

10   Regarding claim 1,

11   Applicant discloses as Admitted Prior Art a computer protection system which

12 utilizes a writing-preventive jumper, applied to a motherboard, in which the writing-

13 preventive jumper ('device') is employed "in order to prevent a computer from being

14 spoiled by some types of virus that are capable of invading a BIOS memory chip to

15 erase the programs thereof," or to prevent a virus from "invading a CMOS chip to

16 rewrite data or the real-time clock chip to result in a booting failure of the computer."

17 (Instant application, par.2, fig. 1).

18   Applicant does not disclose, as Admitted Prior Art, that the write-preventive

19 jumper and motherboard is accommodated by a computer housing. Nor, does the

20 Admitted Prior Art disclose that the write-preventive device is mounted on the computer

21 housing, accessible by the user, and is electrically connected to the BIOS memory chip,

22 the CMOS chip, and the real time clock (RTC) so as to prevent writing to the chips when

23 the writing-preventive device is enabled.

24   Babcock discloses that configuration jumpers located on a computer

25 motherboard are accommodated (enclosed by a system chassis) by a computer

1   housing (Babcock, col. 1, lines 44-63). Babcock discloses that these configuration

2   jumpers, as an example, are used to control or configure operations of the CMOS or

3   BIOS. Babcock discloses that jumpers are electrically connected to their respective

4   input/output ports (Babcock, col. 1, lines 10-28, 44-63). However, Babcock teaches that

5   the use of configuration jumpers on a motherboard are inconvenient, as the user must

6   open the system chassis and access the motherboard in order to manipulate the

7   configuration jumper. Therefore, Babcock teaches that a control device, located on the

8   computer housing (Babcock, col. 3, lines 33-38), can be used to replace the operation

9   or configuration of computer functions via jumpers. The control device is electrically

10 connected to the respective general input/output ports, previously connected to by the

11 jumper, so as to control the configuration of the computer component (Babcock, col. 3,

12 lines 64-67; figs. 1, 2).

13   It would have been obvious to one of ordinary skill in the art to employ the

14 method of Babcock (for replacing a configuration jumper with a control device so as to

15 control the configuration of computer components) with the computer protection system

16 of the Admitted Prior Art. This would have been obvious because one of ordinary skill in

17 the art would have been motivated to allow a user to enable writing-preventive computer

18 protection for the BIOS memory, CMOS, and RTC without the inconvenience of opening

19 the computer and manipulating the writing-preventive jumper.

20   Thus, the combination of the Admitted Prior Art and Babcock discloses a writing

21 preventive device that is applied in a computer, composed of a motherboard and a

22 computer housing for accommodating the motherboard, and is mounted on the

1   computer housing (Babcock, col. 1, lines 44-63; col. 33-38). The writing preventive

2   device is electrically connected with a BIOS memory chip, a real time clock chip, and a

3   CMOS chip. The Admitted Prior Art discloses the functional connection of the jumper to

4   the chips (Instant Application, par. 2), while Babcock further qualifies this connection as

5   comprising an electrical connection (Babcock, col. 3, lines 64-67; figs. 1, 2). In addition,

6   the combination of the Admitted Prior Art and Babcock discloses that the writing-

7   preventive device prevents writing to the chips when enabled (Instant Application, par.

8   2; Babcock, col. 1, lines 44-63).

9

10   Regarding claim 2, the combination of the Admitted Prior Art and Babcock

11   discloses an electrical connection to the chips. The writing-preventive device is

12   disclosed to prevent writing to the chips. It is not specifically disclosed that the writing-

13   preventive device connects to the R/W signal pins of the chips. However, it would have

14   been obvious to one of ordinary skill in the art to connect the writing-preventive device

15   to the R/W signal pins of the chips. This would have been obvious because one of

16   ordinary skill in the art would have been motivated to connect a writing-preventive

17   device to the signal pins associated with writing, so as to prevent writing to the chip.

18

19   Regarding claim 3, the combination of the Admitted Prior Art and Babcock

20   discloses:

21   *at least an on/off control switch mounted on the housing for enabling or disabling*

22   *a data-writing action to said chips* (Instant Application, par. 2; Babcock. cols. 1 – 3).

1

2   Regarding claim 4, the combination of the Admitted Prior Art and Babcock

3 discloses:

4   *in which the on/off control switch is a switch having mechanical contacts*

5 (Babcock, col. 3, lines 33-38).

6

7   Regarding claim 5, the combination of the Admitted Prior Art and Babcock

8 discloses:

9   *in which the on/off control switch is a semiconductor switch* (Babcock, cols. 3, 4;

10 fig. 1). Babcock discloses the switch comprising contacts on an integrated circuit, or

11 semiconductor.

12

13   **Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over the**

14 **combination of the Admitted Prior Art and Babcock as applied to claims 1 – 5**

15 **above, and further in view of Chen, "Infrared Remote Control", U.S. Patent**

16 **Publication 2003/0006904 A1.**

17

18   Regarding claim 6, the combination of the Admitted Prior Art and Babcock does

19 not disclose in which the on/off control switch is an infrared-ray remote control switch.

20   However, Chen teaches for purposes of convenience, devices previously not

21 equipped with remote control switches, may be provided with remote control infrared
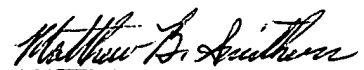
22 switches.

1   It would have been obvious to one of ordinary skill in the art to employ the

2   teaching of Chen for equipping switch-able devices with infrared remote control

3   switches with the computer protection system of the combination of the Admitted Prior

4   Art and Babcock. This would have been obvious because one of ordinary skill in the art

5   would have been motivated to provide a more convenient way to operate the switching

6   mechanism of the present invention.

7

8   ***Conclusion***

9

10   The following prior art made of record and not relied upon is considered pertinent

11 to applicant's disclosure:

12   Largman et al., "Computer with Switchable Components", U.S. Patent Publication

13 2002/0188887 A1.

14   Kao et al., "Method of Protecting Basic Input/Output System", U.S. Patent

15 Publication 2003/0126459.

16   James et al., "Method for Restoring CMOS in a Jumperless System", U.S. Patent

17 6,647,512 B1.

18   Zimmer et al., "Method and System Using a Virtual Lock for Boot Block Flash",

19 U.S. Patent Publication 2002/0144050 A1.

20

21   A shortened statutory period for reply is set to expire **3 months** (not less than 90

22 days) from the mailing date of this communication.

1   Any inquiry concerning this communication or earlier communications from the

2   examiner should be directed to Jeffery Williams whose telephone number is (571) 272-

3   7965. The examiner can normally be reached on 8:30-5:00.

4   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

5   supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone

6   number for the organization where this application or proceeding is assigned is (703)

7   872-9306.

8   Information regarding the status of an application may be obtained from the

9   Patent Application Information Retrieval (PAIR) system. Status information for

10 published applications may be obtained from either Private PAIR or Public PAIR.

11 Status information for unpublished applications is available through Private PAIR only.

12 For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

13 you have questions on access to the Private PAIR system, contact the Electronic

14 Business Center (EBC) at 866-217-9197 (toll-free).

15

16
17 Jeffery Williams
18 Assistant Examiner
19 Art Unit 2137
20 571.272.7965
21 07.06.2005

MATTHEW SMITHERS
PRIMARY EXAMINER
Art Unit 2137